Record Power-Added-Efficiency, Low-Voltage GOI (GaAs On Insulator) MESFET Technology for Wireless Applications

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***Abstract*— A record-high power-added efficiency (PAE) is obtained from a GaAs on insulator (GOI) MESFET. Al_2O_3 obtained by the wet oxidation of $Al_{0.98}GaAs$ in steam is used as the insulating buffer layer. The insulating buffer results in elimination of buffer leakage and enhanced charge control. 0.35-μm gate-length GOI MESFET's exhibiting a record PAE of 72% at a drain voltage of 3 V at 4 GHz are demonstrated.**

***Index Terms*— GaAs transistor, high efficiency, insulating buffer, low voltage, MESFET, wireless technology.**

I. Introduction

MICROWAVE power amplifiers are fundamental components for wireless mobile communication, satellite and space technology, and phased-array radar applications. Output power, efficiency, linearity, and large signal gain are the most important characteristics of a microwave power amplifier. Higher efficiency would allow for lighter and smaller power sources, reduced cooling requirements and increased operating time. Low drain bias operation is highly desirable for wireless handset applications, as lighter and smaller batteries can be used making the module compact. While GaAs- and InP-based high electron-mobility transistors (HEMT's) [1] and heterojunction bipolar transistors (HBT's) [2] are viable candidates for these needs, GaAs MESFET's are very attractive due to their relative simplicity and lower cost [3]. We have developed GaAs on insulator (GOI) devices for a high-efficiency and linearity technology [4]. Al_2O_3 obtained by the wet oxidation of $Al_xGa_{1-x}As$ in steam [5] is used as the insulating buffer layer, which results in the elimination of substrate leakage current leading to higher output resistance and improvement in the pinchoff characteristics. This gets translated to high-efficiency operation as a power amplifier. This is so as the substrate leakage in an FET is a component of the total current that does not get modulated by the gate, it directly translates to lost power and, hence, reduced efficiency. At 4 GHz, power-added efficiency (PAE) of 67.7% at a low drain bias of 3 V, with output power 75 mW/mm was obtained. With harmonic tuning [6], a PAE of 72% was achieved. To the best of our knowledge, this is the highest reported PAE for a GaAs MESFET under these conditions.

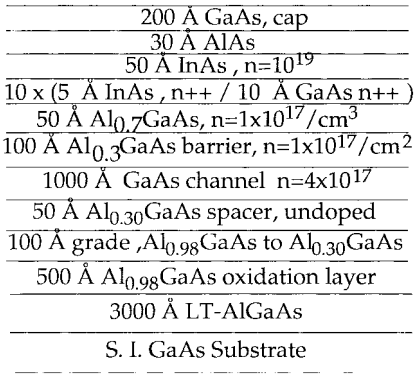

Fig. 1. Epitaxial layer structure of the GOI MESFET.

II. GOI MESFET Fabrication

The epilayer structure and device schematic of the GOI MESFET is shown in Figs. 1 and 2, respectively. The LT-AlGaAs layer below the buffer layer insulator serves as a getterer for Arsenic released during oxidation and helps in minimizing any charge depletion resulting from oxidation [5]. The undoped GaAs cap layer protects the active device from any unwanted oxidation from the top. The fabrication starts with mesa isolation by $BCl_3/Cl_2/SiCl_4$-based reactive ion etching, simultaneously exposing the $Al_{0.98}GaAs$ buffer layer from the side. Next is the lateral wet oxidation of the $Al_{0.98}GaAs$. The oxidation is done in steam, which is introduced into a quartz furnace maintained at the desired oxidation temperature (420 °C) by means of nitrogen carrier gas bubbling through water at 85 °C (see Fig. 3).

After this, the GaAs cap and thin AlAs etch stop layers are removed using selective citric-acid-based etching

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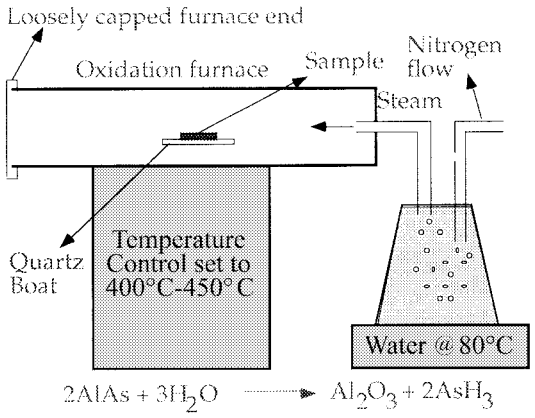


Fig. 2. Oxidation furnace schematic.

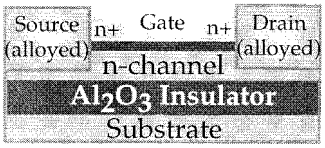


Fig. 3. GOI MESFET schematic.

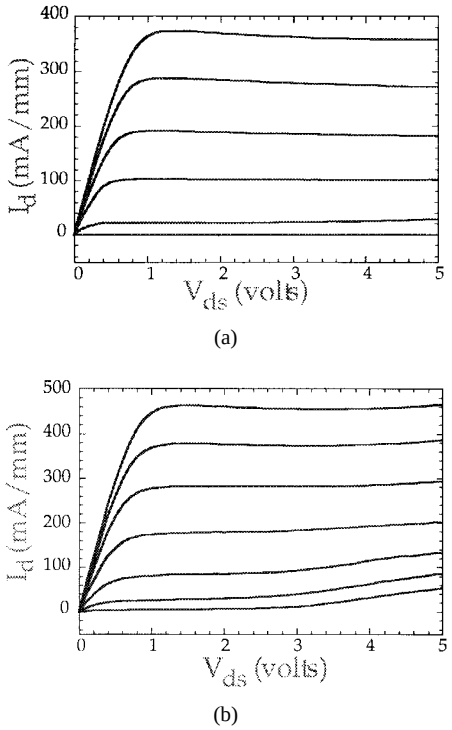


Fig. 4. Drain *I–V* characteristics. (a) GOI. ($V_{\rm gs} = 0.5V$ to -2 V, step $= -0.5$ V.) (b) Control MESFET's ($V_{\rm gs} = 0.5V$ to -2.5 V, step $= -0.5$ V).

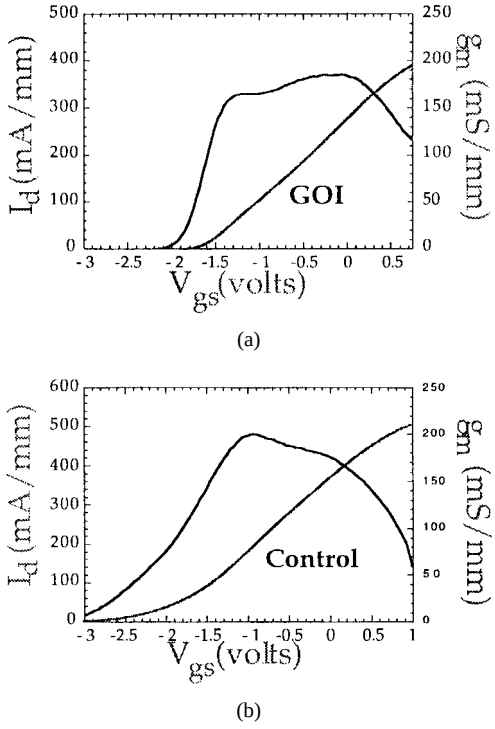


Fig. 5. Transconductance characteristics of (a) GOI and (b) control MESFET's ($V_{\rm ds} = 3$ V).

and phosphoric-acid-based etching, respectively. Then, Ni/Ge/Au/Ni/Au contacts are evaporated and alloyed to form the source and drain regions. Next, the 0.35-μm T-gates are written by E-beam lithography (E-beam lithography performed at Hughes Research Laboratories (HRL), Malibu, CA). Recess etching is done by selective citric-acid-based etchant. Ti/Pt/Au Schottky metallization completes the device. Control MESFET's are also fabricated in the same fashion, except that the oxidation step is omitted.

III. Results and Discussion: DC and Small-Signal RF Measurements

The dc *I–V* characteristics of the GOI (oxidized buffer) and the control MESFET are shown in Fig. 4(a) and (b). The devices have a gate length of 150 μm. As evident, the oxidized buffer results in a lower output conductance and also better pinchoff characteristics due to the elimination of substrate leakage. The $I_{\rm dss}$ (channel current at $V_{\rm gs} = 0$) of the GOI MESFET is 280 mA/mm and that of the control MESFET is 380 mA/mm. The slight current reduction comes about due to back depletion at the oxide-channel interface. However, this has been minimized to about 100 mA/mm, much lower than the previous observed values of over 300 mA/mm [4], which is due to the As gettering effect of the LT AlGaAs buffer. Assuming an electron velocity of 1×10^7 cm/s, this current depletion corresponds to a charge density in the $10^{11}/\text{cm}^2$ range at the oxide semiconductor interface. The nominal two-terminal gate–drain diode breakdown voltage was around 10.5 V, defined at 1 mA/mm of reverse bias current.

From the transconductance characteristics of Fig. 5(a) and (b), it is clear that the insulating buffer results in much sharper g_m characteristics near pinchoff. This is due to the elimination of substrate leakage. A higher g_m near pinchoff simultaneously with sharper turnoff characteristics serves to improve both the efficiency and linearity when the device is used as a power amplifier [7].

S-parameter measurements were done on an HP 8510B network analyzer. The short-circuit current gain cutoff frequency f_t and the maximum oscillation frequency $f_{\rm max}$ were

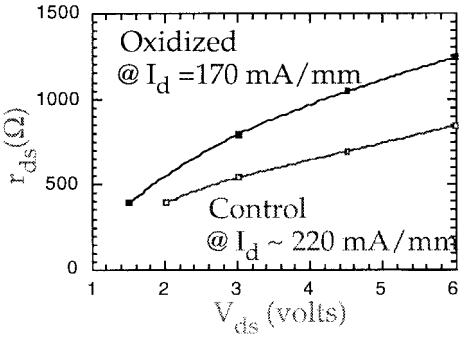


Fig. 6. Extracted RF output resistance for the GOI and control devices.

determined to be 22 GHz/75 GHz (GOI, $I_d = 168$ mA/mm) and 23 GHz/67 GHz (control, $I_d = 178$ mA/mm) at $V_{\rm ds} = 3$ V. The f_t's are similar as expected, indicating that electron velocity is unaffected by the oxidation process. The $f_{\max}$ of the oxidized device is higher due to an improvement in $r_{\rm ds}$. The extracted RF output resistance (from s-parameter data) for the oxidized and control device is shown in Fig. 6. It is clear that the improvement in output resistance in the GOI device is not merely a dc phenomena, but is also obtained at higher frequencies. The increased output resistance helps to improve the $f_{\max}/f_t$ ratio, as seen from the following relation:

$$f_{\max} = \frac{f_\tau}{2\sqrt{\dfrac{r_i + r_g + r_s}{r_{\rm ds}} + 2\pi f_\tau r_g c_{\rm gd}}}.$$

IV. Results and Discussion: Large-Signal Power, Efficiency, and Linearity Measurements

Power and efficiency measurements were performed at 4 GHz using the ATN LP1 load–pull system. The GOI device had an efficiency of 67.7% at a low drain bias of 3 V with an associated output power of 75 mW/mm; under class-B ($I_d = 2$ mA) biasing conditions, as shown in Fig. 7(a). The highest efficiency obtainable from the control device [Fig. 7(b)] was 58% under similar conditions ($V_{\rm ds} = 3$ V, $I_d = 3$ mA), which was considerably lower than the GOI sample. Low drain-bias operation, as said earlier, is crucial for wireless handset applications.

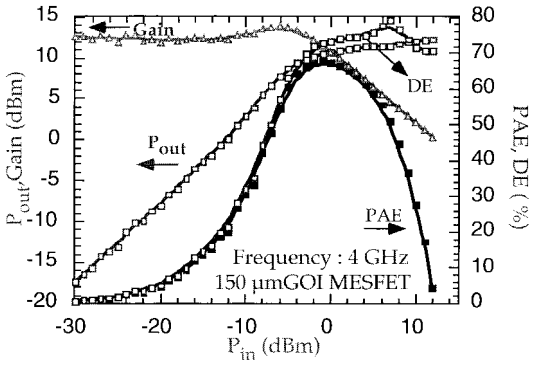
The GOI device performed very well even with an ultra-low drain bias of 1.5 V, with a PAE of 57% and $P_{\rm out}$ of 30 mW/mm. All the measurements were optimized for maximum efficiency. When optimized for maximum power, the gain in power was around 1 dB, but the corresponding drop in efficiency was around 5%–10%. Near Class-A operation for the GOI MESFET ($V_{\rm ds} = 5$ V, $I_d = 200$ mA/mm) resulted in a $P_{\rm out}$ of 335 mW/mm with a peak PAE of 48%. The maximum saturated power was 420 mW/mm (18 dBm) These results are shown in Fig. 8.

For the given load match, with $\Gamma_L = 0.57$, the resistance R can be calculated to be 183 Ω as follows:

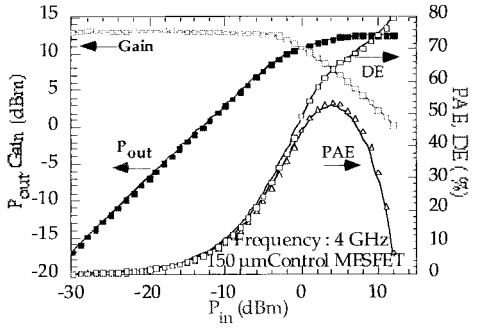
$$\frac{Z_L}{Z_0} = \frac{1+\Gamma_L}{1-\Gamma_L}$$

where Z_0 is 50 Ω. Since R is also the slope of the load line,

$$\Delta V/\Delta I = R = 183\ \Omega$$



(a)



(b)

Fig. 7. Power and efficiency measurements for 0.35 μm × 150 μm (a) GOI and (b) control MESFET's. (Source: $\Gamma_s = 0.77\angle 21.6$, load state: $\Gamma_1 = 0.78\angle 8$.)

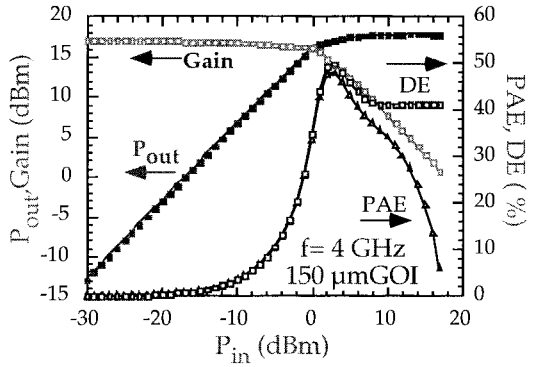


Fig. 8. Near Class-A measurements for the GOI MESFET. (Source: $\Gamma_s = 0.65\angle 16.3$, load state: $\Gamma_1 = 0.57\angle 6.6$.)

Since the biasing is near Class-A, the output power is given as

$$P_{\rm out} = \tfrac{1}{8}\Delta V \Delta I = 50\ \text{mW}$$

where ΔV and ΔI are the large-signal voltage and current swings. From the above relations, $\Delta V = 8.5$ V, and $\Delta I = 46$ mA (or 306 mA/mm). The theoretical expected voltage and current swings (for perfect Class-A operation) can be estimated from the dc *I–V* characteristics of Fig. 4(a) and (b) as

$$\Delta V = V_{bd} - V_k = 9 - 1 = 8\ \text{V}$$
$$\Delta I = I_{\max}\ (\text{at } V_{\rm gs} = 0.5\ \text{V}) = 350\ \text{mA/mm}.$$

The close agreement of these numbers; calculated from the measured power performance and expected from the dc char-

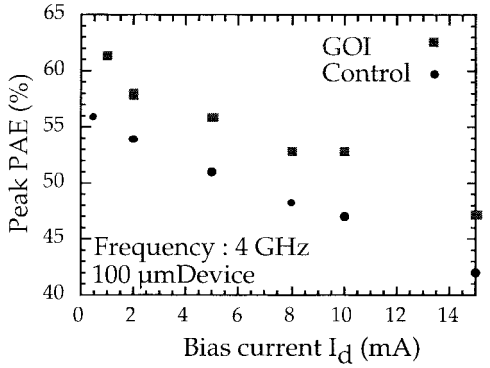


Fig. 9. Peak PAE as a function of bias condition.

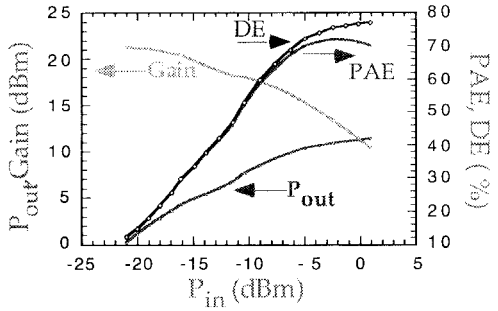


Fig. 10. Active load–pull measurements with harmonic matching for the GOI MESFET. ($V_{\rm ds}$ = 3 V, I_d = 3 mA. Load state: $\Gamma_L = 0.79\angle 9$, fundamental: 4 GHz, 150-μm GOI MESFET.)

acteristics, demonstrate that there is a close match between the dc and large signal RF performance with the GOI technology.

Power measurements were also done for 100-μm-wide devices. The $I_{\rm dss}$ of the GOI and control devices was 27 and 39 mA, respectively. The maximum PAE for both the device is compared as a function of the bias condition (Fig. 9). The bias is varied from Class-B, through Class-AB toward Class-A. Clearly, the GOI device is superior to the control device over the entire bias range.

Active Load–Pull Measurements with Harmonic Matching

Providing the optimum loads at the harmonics can lead to an improvement in efficiency [6] Active load–pull measurements [8] with harmonic matching were done at Hughes Space and Communication. With a near short circuit at the second harmonic and a near open circuit at the third harmonic, a PAE of 72% (Fig. 10) at an output power level of 85 mW/mm at 4 GHz with $V_{\rm ds}$ of 3 V was achieved. The third harmonic termination was near open circuit, while the second harmonic termination was near short circuit. To the best of our knowledge, these results represent the highest reported PAE for a GaAs-based MESFET operating under the above conditions.

Linearity Measurements

A power amplifier for wireless applications has to satisfy stringent linearity specifications depending on the system it is used in. This makes it very important to have an estimate on the linearity performance of our GOI MESFET's. The linearity measurements are done in collaboration with Wright Patterson

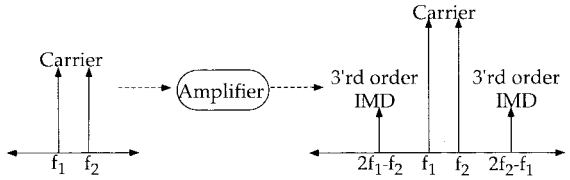


Fig. 11. Principle of two-tone third-order IMD distortion.

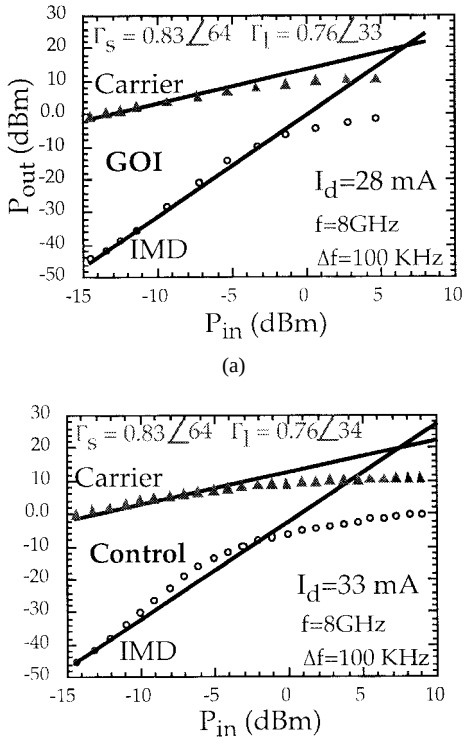


Fig. 12. IP_3 measurements at 8 GHz with 100-kHz offset.

Air Force Base Laboratories, Dayton, OH, using the system from Maury microwave. We performed two-tone IMD measurements at 8 GHz. The two tones f_1 and f_2 are separated by 100 kHz. The basic principle of two-tone IMD measurement is shown in Fig. 11. The third-order nonlinearities result in the unwanted products near the signal frequency in the output as shown. The IMD is a measure of how much below the carrier output power are these third-order terms. An intermodulation product termed as IP_3 can be defined as the power level when the carrier power becomes equal to the third-order IMD power, as shown in Fig. 12(a) and (b), which plot the results of IMD measurements for both the samples at $V_{\rm ds}$ = 3 V. The IP_3 product is similar in both samples, around 20 dBm. In general, if the IP_3 is 10 dBm above the 1-dB saturated power, the amplifier is considered to be fairly linear. The GOI technology satisfies this criterion, simultaneously obtaining high efficiency. The carrier-to-intermodulation separation is slightly higher in the GOI sample.

V. Conclusion

We presented the dc, RF, and large-signal performance data for the submicron GOI technology. It is demonstrated

the advantage gained by the insulating buffer by eliminating substrate leakage current is reflected in the dc, RF, and power performance of the GOI MESFET's with respect to the control MESFET's. Submicrometer GOI MESFET's with world-record efficiencies were fabricated. The highest PAE obtained was 72% (with harmonic matching) at 4 GHz, at a low drain bias of 3 V, the highest reported under these conditions, to the best of our knowledge. We expect similar performance improvements in wider gatewidth devices, on which some of the future efforts will be focussed. 1.5-V operation was also demonstrated with a PAE of 57%. While more detailed measurements on linearity of the devices are required, initial IMD measurements show that the GOI MESFET's have a fairly decent linearity performance with IP_3 about 20 dBm, 10 dBm higher than the saturated 1-dB output power. A technology that can obtain high efficiency with high linearity at low supply voltages would be an ideal choice for wireless applications, and the GOI technology satisfies this requirements. This performance is achieved by the insulating buffer, which results in elimination of substrate leakage, better pinchoff characteristics, and improved charge control.

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Dr. Mishra was awarded the Young Scientist of the Year Award by the International Symposium on GaAs and Related Compounds. He is the recipient of a Hyland Patent Award, which is presented by Hughes Aircraft.

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Mr. Jenkins is a member of Tau Beta Pi, Eta Kappa Nu, and Phi Kappa Ph.